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EXAMINER	
VERDERAMO III, RALPH	
ART UNIT	**PAPER NUMBER**
2186	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/821,712	LANDIN ET AL.	
	Examiner	Art Unit	
	Ralph A. Verderamo III	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 3 and 41 recites the limitation "the first coherency unit". There is insufficient antecedent basis for this limitation in these claims. The limitation "the first coherency unit" is used without first describing "a first coherency unit". Furthermore "the first coherency unit" implies that there will be multiple coherency units however in later dependent claims only the term "the coherency unit" is used.

3. Claim 49 recites the limitations "the first means for communicating address packets" in lines 20 – 21 and "the first coherency unit" in line 26. There is insufficient antecedent basis for these limitations in the claim. The limitation "the first means for communicating address packets" is used without first describing "a first means for communicating address packets".

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1 – 10, 12 – 23, 25 – 37, 39 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Singhal et al. US Patent No. 5978874 (herein after referred to as Singhal) in view of Frank et al. US Patent No. 5251308 (herein after referred to as Frank).

Regarding claims 1, 13, 28 and 49, Singhal describes a system, comprising: an inter-node network configured to communicate coherency messages (Network 20, FIG. 1. Coherency messages are sent between boards (nodes) on the network (column 14, lines 28 – 52)); a node coupled to the inter-node network and including a plurality of devices (board 50-1 of FIG. 1 and board 50-N of FIG. 2) and an address network configured to convey address packets between the plurality of devices (The address paths of FIG. 2 connecting address controller 180 to devices 150-N, 160-N and 170-N forms an address network (column 6, lines 30 – 34)), wherein the plurality of devices includes an active device (UPA device 160-N of FIG. 2), a memory subsystem (Memory 150-N of FIG. 2), and an interface configured to send and receive coherency messages on the inter-node network (Address controller 180 and bit-sliced data buffer 140 of FIG. 2 form the interface to the inter-node network described above); an additional node coupled to the inter-node network (board 50-2 of FIG. 1) and configured to send on the inter-node network a coherency message requesting

an access right to a coherency unit (A board requests ownership (an access right) by initiating a ReadToOwn transaction (column 14, lines 18 – 39)); wherein in response to receiving the coherency message via the inter-node network, the interface is configured to send a proxy address packet on the address network (According to the description of Read-Type transactions (column 12, line 47 – column 13, line 5) all boards (nodes) communicate with the address bus and snoop on that address. This means the interface is responding to a message from the inter-node network and causing the board (node) to check its own memory for the requested address); wherein in response to the proxy address packet, the memory subsystem is configured to provide the interface with data corresponding to the coherency unit (the data is loaded into the destination (column 13, line 5)) and an indication of a global access state of the coherency unit in the node (All boards drive State Signals indicating the state of the line at the time when the address was on the address bus (column 12, lines 55 – 57)). Singhal does not specifically describe wherein if the active device is an owner of the coherency unit, the active device is configured to ignore the proxy address packet.

Frank, which describes a shared memory in a multiprocessor system, discloses a mode of operation in which requests to a datum by a second CPU are ignored if that datum is anchored to a first CPU (exclusively owned by the first CPU) (column 3, lines 7 – 26).

It would have been obvious to one of ordinary skill in the art at the time of the invention to include the anchoring of Frank with the invention of Singhal because Frank teaches that providing the ability to anchor data affords greater program control of data movement in the system (column 4, lines 21 – 26).

Regarding claim 2, Singhal in view of Frank describe the system of claim 1 (see above). Furthermore Singhal describes that the additional node includes an additional plurality of devices and an additional address network configured to convey address packets between the additional plurality of devices, wherein the additional plurality of devices includes an additional active device and an additional interface configured to send and receive coherency messages on the inter-node network, wherein the additional interface is configured to send the coherency message on the inter-node network in response to the active device sending a packet requesting an access right to the coherency unit on the additional address network (Board (node) 50-2 of FIG. 1 and FIG. 2 shows the additional devices, additional interface and additional address network within the board (node) as described with respect to claim 1 above).

Regarding claims 3, 14 and 29, Singhal in view of Frank describe the system of claim 2 (and the node of claim 13) (and the method of claim 28) (see above), wherein the coherency message requests a read access right to the first coherency unit, wherein the proxy address packet is a proxy memory read packet (A board (node) requests ownership (an access right) by initiating a ReadToOwn transaction (Singhal, column 14, lines 18 – 39). ReadToOwn is a read access

right. Furthermore according to the description of Read-Type transactions (Singhal, column 12, line 47 – column 13, line 5) all boards (nodes) communicate with the address bus and snoop on that address. This means the interface is responding to a message from the inter-node network and causing the board (node) to check its own memory for the requested address which would require the use of the address network. As stated before since it a read command has been described the request would be a proxy memory read packet).

Regarding claims 4, 15 and 31, Singhal in view of Frank describe the system of claim 3 (and the node of claim 14) (see above) (and the method of claim 30) (see claim 30 below), wherein if the indication provided by the memory subsystem indicates that the global access state of the coherency unit in the node is a modified state, the interface is configured to responsively send a proxy read-to-share-modified address packet on the address network (As described in the application a proxy read to share modified is just a read transaction that requests an access right to a modified coherency unit (page 68, paragraph [00189]). Singhal describes determining if a cache line is in a modified state (column 24, lines 5 – 9) and furthermore a proxy read to share modified address packet would occur if that modified cache line were requested).

Regarding claims 5, 16 and 32, Singhal in view of Frank describe the system of claim 4 (and the node of claim 15) (and the method of claim 31) (see above), wherein if the active device is the owner of the coherency unit, the active device is configured to send data corresponding to the coherency unit to the

interface in response to receipt of the proxy-read-to-share-modified packet (The data is loaded into the destination (Singhal, column 13, line 5). As described the data is loaded into the requesting destination by the responding board (node) which is the board (node) that owns the requested data).

Regarding claims 6,17 and 33, Singhal in view of Frank describe the system of claim 5 (and the node of claim 15) (and the method of claim 31) (see above), wherein if the active device is the owner of the coherency unit, the active device is configured to transition an ownership responsibility for the coherency unit upon receipt of the proxy read-to-share-modified packet (ReadToOwn transaction (Singhal, column 14, lines 53 – 66) describes how the initiator is given ownership of the cache line and the current owner (the responder) invalidates its own copy of the cache line giving the initiator exclusive ownership).

Regarding claims 7, 20 and 34, Singhal in view of Frank describe the system of claim 2 (and the node of claim 13) (and the method of claim 28) (see above), wherein the coherency message requests a write access right to the coherency unit, wherein the proxy address packet is a proxy read-to-own packet (The ReadToOwn transaction is used to satisfy cache write misses (Singhal, column 14, lines 18 – 27)).

Regarding claims 8, 21 and 35, Singhal in view of Frank describe the system of claim 7 (and the node of claim 20) (and the method of claim 34) (see above), wherein the plurality of devices includes an other active device (UPA device 160-N of FIG. 2 which would be on board (node) 50-2 of FIG. 1), wherein

if the other active device has a read access right to the coherency unit, the other active device is configured to transition the read access right to an invalid access right upon receipt of the proxy read-to-own packet (The cache line owner invalidates its copies of the line (Singhal, column 14, lines 57 – 60)).

Regarding claims 9, 22 and 36, Singhal in view of Frank describe the system of claim 7 (and the node of claim 20) (and the method of claim 34) (see above), wherein if the indication provided by the memory subsystem indicates that the global access state of the coherency unit in the node is a modified state, the interface is configured to responsively send a proxy read-to-own- modified address packet on the address network (As described in the application a proxy read to own modified is just a write transaction that requests an access right to a modified coherency unit (page 68, paragraph [00189]). Singhal describes determining if a cache line is in a modified state (column 24, lines 5 – 9) and furthermore a proxy read to own modified address packet would occur if that modified cache line were requested).

Regarding claims 10, 23 37, Singhal in view of Frank describe the system of claim 9 (and the node of claim 22) (and the method of claim 36) (see above), wherein if the active device is the owner of the coherency unit, the active device is configured to transition an ownership responsibility for the coherency unit upon receipt of the proxy read-to-own-modified packet and to send data corresponding to the coherency unit to the interface in response to receipt of the proxy- read-to-own-modified packet, wherein the active device transitions an access right to the

coherency unit upon sending the data (The initiator assumes ownership of the cache line while the previous cache line owner invalidates its copies of the cache line and responds to the initiator with the data (Singhal, column 14, lines 53 – 60)).

Regarding claims 12, 25 and 39, Singhal in view of Frank describe the system of claim 2 (and the node of claim 13) (and the method of claim 28) (see above), wherein the address network is configured to convey the proxy address packet from the interface to the plurality of devices in broadcast mode (An Address Bus is used to broadcast commands from a requesting board to all boards in the system (Singhal, column 7, lines 37 – 40)).

Regarding claims 18 and 30, Singhal in view of Frank describe the node of claim 14 (and the method of claim 28) (see above), wherein if the indication provided by the memory indicates that the global access state of the coherency unit in the node is a shared state (All boards snoop on the address bus packet and assert Shared if they have a cached copy of the line (Singhal, column 13, lines 37 – 39)), the interface is configured to communicate the data corresponding to the coherency unit on the inter-node network (If a board (node) owns the requested cache line it responds to the transaction (column 13, lines 50 – 51) by sending data (column 13, line 5)).

Regarding claim 19, Singhal in view of Frank describe the node of claim 13 (see above), wherein the coherency message requests a write access right to the coherency unit (The ReadToOwn transaction is used to satisfy cache write

misses (Singhal, column 14, lines 19 – 21)), wherein in response to the proxy address packet, the memory is configured to update the global access state of the coherency unit in the node (If necessary the boards (nodes) update their cache tags in their board mounted DTAG RAM (memory) (column 12, lines 53 – 61)).

Regarding claim 26, Singhal in view of Frank describe the node of claim 13 (see above), wherein the interface includes a global access state cache indicating the global access states of a plurality of recently accessed coherency units in the node (The state of every cache line in the distributed memory system is stored (Singhal, column 22, lines 58 – 62)).

Regarding claim 27, Singhal in view of Frank describe the node of claim 26 (see above), wherein the interface is configured to check the global access state cache for the global access state of the coherency unit in the node, wherein if the global access state of the coherency unit in the node is not included in the global access state cache, the interface is configured to send the proxy address packet to the memory (This represents a miss in all the cache lines and would appropriately be handled by finding the requested line in main memory and then updating its state).

4. Claims 11, 24 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Singhal in view of Frank as applied to claim 2 above, further in view of Ekanadham et al. US Patent No. 6085295 (herein after referred to as Ekanadham).

Regarding claims 11, 24 and 38, Singhal in view of Frank describe the system of claim 2 (and the node of claim 13) (and the method of claim 28) (see above). Singhal in view of Frank do not describe that the address network being configured to convey the proxy address packet from the interface to a directory in point-to-point mode.

Ekanadham, which describes keeping data coherency between nodes, discloses that in order to support bigger and faster networks of nodes the network must be transitioned from being bus based to switch based which requires point-to-point transactions (column 1, lines 44 – 58).

It would have been obvious to one of ordinary skill in the art at the time of the invention to include the point-to-point interconnection of a switch based network as described by Ekanadham with the invention of Singhal in view of Frank because Ekanadham teaches that switch based networks allow for faster and bigger node networks (column 1, lines 44 – 58).

5. Claims 40, 41 and 45 – 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Singhal in view of Frank, Slaughter US Patent No. 6058400 (herein after referred to as Slaughter) and Young et al. US Patent No. 5809536 (herein after referred to as Young).

Regarding claim 40, Singhal describes a system, comprising: a node including a plurality of devices (board 50-1 of FIG. 1 and board 50-N of FIG. 2) and an address network configured to convey address packets between the plurality of devices (The address paths of FIG. 2 connecting address controller

180 to devices 150-N, 160-N and 170-N forms an address network (column 6, lines 30 – 34)), wherein the plurality of devices includes an active device (UPA device 160-N of FIG. 2), a memory subsystem (Memory 150-N of FIG. 2), and an interface to an inter-node network (Address controller 180 and bit-sliced data buffer 140 of FIG. 2 form the interface to the inter-node network described above); an additional node (board 50-2 of FIG. 1) coupled to send the node a coherency message requesting an access right to a coherency unit via the inter-node network (A board requests ownership (an access right) by initiating a ReadToOwn transaction (column 14, lines 18 – 39)); wherein in response to the type of proxy address packet, the memory subsystem is configured to provide the interface with data corresponding to the coherency unit (the data is loaded into the destination (column 13, line 5)) and an indication of a global access state of the coherency unit in the node (All boards drive State Signals indicating the state of the line at the time when the address was on the address bus (column 12, lines 55 – 57)). Singhal does not specifically describe there being a plurality of types of proxy address packets, one of which is sent dependent on a global access state of the coherency unit wherein if the interface does not have an indication of the global access state of the coherency unit in the node the interface is configured to send a type of proxy address packet associated with a shared global access state. Singhal also does not describe the active device being configured to ignore the type of proxy address packet if the active device is an owner of the coherency unit.

Slaughter, which describes a cluster coherent file system, discloses that different actions are taken if it is determined that the coherency unit is in certain coherency states. If the coherency unit is modified the slave node must transfer the data to the requesting unit, change the coherency state to invalid and send an acknowledge signal. However if the coherency unit is shared the slave just changes the state to invalid and sends an acknowledge signal (column 10, lines 17 – 55). Since different actions are taken different commands must be used which are based on the state of the data.

It would have been obvious to one of ordinary skill in the art at the time of the invention to include Slaughter's different requests sent based on state of a coherency unit with the invention of Singhal because Slaughter teaches that his system creates a highly-available cluster coherent file-system (column 3, lines 5 – 7).

Young, which describes a cache coherency system, discloses that there is a default state (which could be a shared state (column 2, lines 21 – 24)) to which the cache lines default. This being the case if a cache line's state could not be determined it would be obvious to use a shared access command since that is the default state.

It would have been obvious to one of ordinary skill in the art at the time of the invention to include the default state of Young with the invention of Singhal in view of Slaughter because Young teaches his method reduces the number of coherency operations (column 2, lines 36 – 37).

Frank, which describes a shared memory in a multiprocessor system, discloses a mode of operation in which requests to a datum by a second CPU are ignored if that datum is anchored to a first CPU (exclusively owned by the first CPU) (column 3, lines 7 – 26).

It would have been obvious to one of ordinary skill in the art at the time of the invention to include the anchoring of Frank with the invention of Singhal in view of Slaughter and Young because Frank teaches that providing the ability to anchor data affords greater program control of data movement in the system (column 4, lines 21 – 26).

Regarding claim 41, Singhal in view of Frank, Slaughter and Young describe the system of claim 40 (see above), wherein the coherency message requests a read access right to the first coherency unit, wherein the proxy address packet is a proxy memory read packet (A board (node) requests ownership (an access right) by initiating a ReadToOwn transaction (Singhal, column 14, lines 18 – 39). ReadToOwn is a read access right. Furthermore according to the description of Read-Type transactions (Singhal, column 12, line 47 – column 13, line 5) all boards (nodes) communicate with the address bus and snoop on that address. This means the interface is responding to a message from the inter-node network and causing the board (node) to check its own memory for the requested address which would require the use of the address network. As stated before since it a read command has been described the request would be a proxy memory read packet).

Regarding claim 45, Singhal in view of Frank, Slaughter and Young describe the system of claim 40 (see above), wherein the coherency message requests a write access right to the coherency unit, wherein the proxy address packet is a proxy read-to-own packet (The ReadToOwn transaction is used to satisfy cache write misses (Singhal, column 14, lines 18 – 27)).

Regarding claim 46, Singhal in view of Frank, Slaughter and Young describe the system of claim 45 (see above), wherein the plurality of devices includes an other active device (UPA device 160-N of FIG. 2 which would be on board (node) 50-2 of FIG. 1), wherein if the other active device has a read access right to the coherency unit, the other active device is configured to transition the read access right to an invalid access right upon receipt of the proxy read-to-own packet (The cache line owner invalidates its copies of the line (Singhal, column 14, lines 57 – 60)).

Regarding claim 47, Singhal in view of Frank, Slaughter and Young describe the system of claim 46 (see above), wherein if the indication provided by the memory subsystem indicates that the global access state of the coherency unit in the node is a modified state, the interface is configured to responsively send a proxy read-to-own- modified address packet on the address network (As described in the application a proxy read to own modified is just a write transaction that requests an access right to a modified coherency unit (page 68, paragraph [00189]). Singhal describes determining if a cache line is in a

modified state (column 24, lines 5 – 9) and furthermore a proxy read to own modified address packet would occur if that modified cache line were requested).

Regarding claim 48, Singhal in view of Frank, Slaughter and Young describe the system of claim 47 (see above), wherein if the active device is the owner of the coherency unit, the active device is configured to transition an ownership responsibility for the coherency unit upon receipt of the proxy read-to-own-modified packet and to send data corresponding to the coherency unit to the interface in response to receipt of the proxy- read-to-own-modified packet, wherein the active device transitions an access right to the coherency unit upon sending the data (The initiator assumes ownership of the cache line while the previous cache line owner invalidates its copies of the cache line and responds to the initiator with the data (Singhal, column 14, lines 53 – 60)).

6. Claims 42 – 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Singhal in view of Frank, Slaughter and Young as applied to claim 41 above, further in view of Bailey et al. US Patent No. 5909180 (herein after referred to as Bailey).

Regarding claim 42, Singhal in view of Frank, Slaughter and Young describe the system of claim 41 (see above). They do not describe detecting an incorrect message has been sent and resending a correct message.

Bailey, describes communications between microcomputers, discloses that error detection and error correction is preferably included to prevent the interface from executing an incorrect command. If an erroneous message is

received the protocol detects the error and corrects it in a subsequent message (column 17, lines 44 – 64).

It would have been obvious to one of ordinary skill in the art to include the error detection and correction of Bailey with the invention described by Singhal in view of Frank, Slaughter and Young because Bailey teaches that his protocol prevents execution of incorrect commands (column 17, lines 44 – 64).

Regarding claim 43, Singhal in view of Frank, Slaughter, Young and Bailey describe the system of claim 42 (see above), wherein if the active device is the owner of the coherency unit, the active device is configured to send data corresponding to the coherency unit to the interface in response to receipt of the proxy-read-to-share-modified packet (The data is loaded into the destination (Singhal, column 13, line 5). As described the data is loaded into the requesting destination by the responding board (node) which is the board (node) that owns the requested data).

Regarding claim 44, Singhal in view of Frank, Slaughter, Young and Bailey describe the system of claim 43 (see above), wherein if the active device is the owner of the coherency unit, the active device is configured to transition an ownership responsibility for the coherency unit upon receipt of the proxy read-to-share-modified packet (ReadToOwn transaction (Singhal, column 14, lines 53 – 66) describes how the initiator is given ownership of the cache line and the current owner (the responder) invalidates its own copy of the cache line giving the initiator exclusive ownership).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ralph A. Verderamo III whose telephone number is (571) 270-1174. The examiner can normally be reached on M-Th 7:30 - 5, every other Friday 7:30-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ralph A. Verderamo III
Examiner
Art Unit 2186

rv
February 28, 2007

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
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